EENG 414: ASIC design using CAD

QPSK channel coding in WiMAX physical layer

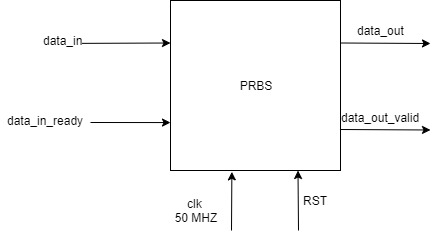
Project Design Document

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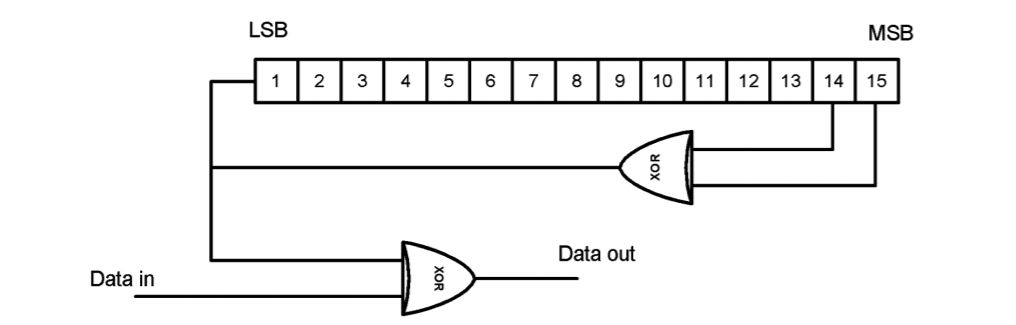
Randomizer:

1-block diagram:



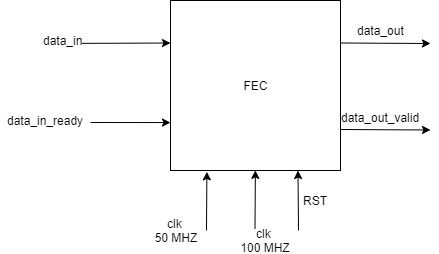
2-Description:

For every input the prbs block receives, it produces 1 output corresponding to this

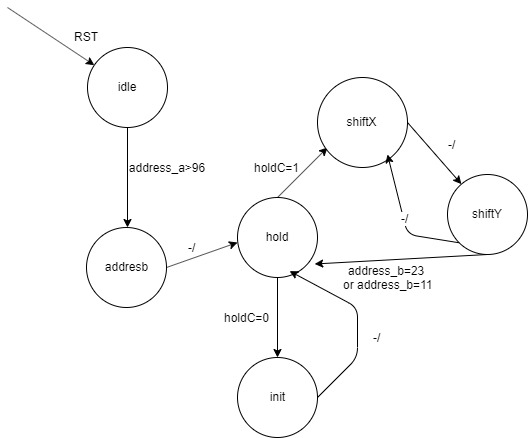


FEC encoder:

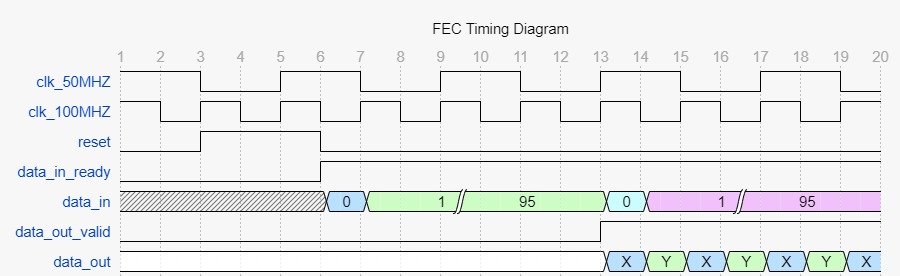
1-Block diagram



2-FSM



3-timing diagram:

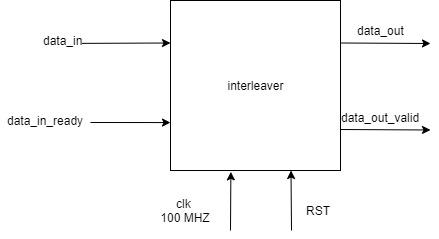


4- description:

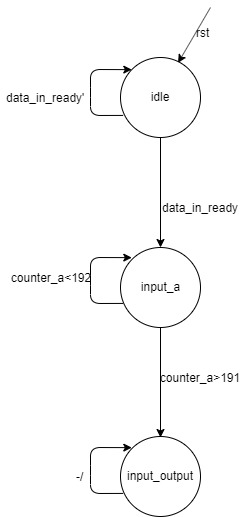
The data is encoded using tailbiting convolutional coding which is implemented through the finite state machine. The first block is stored in a DPR and is processed while the second block is being loaded into the DPR.

Interleaver

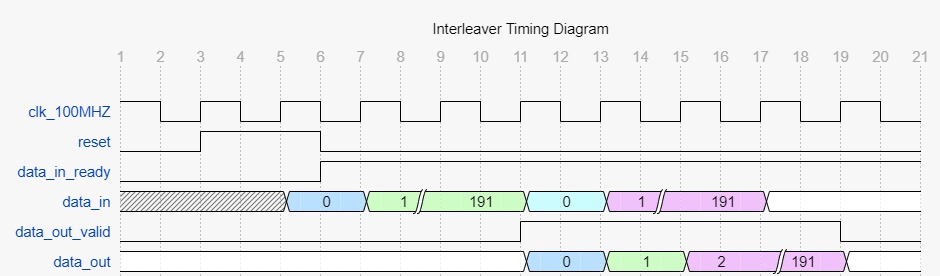
1- Block diagram:



2-FSM



3-timing Diagram

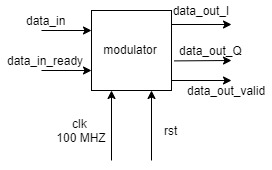


4-description

Bit interleaving is done by processing the new index of the incoming bits and placing them inside a DPR with the new index. The output is then read through the second port of the DPR.

Modulator:

1-Block diagram



2-timing diagram

